IQS7219A DATASHEET

A Versatile Proximity Sensing Device for High Performance and Low Power Application. The device is focused on proximity and touch applications with direct output requirements. Up to 2 channels can be configured in a range of available sensing modes

1 Device Overview

1.1 Main Features

- Highly flexible ProxFusion® device
- 2 configurable channels
  - Each channel can pair multiple sensor connections. (see Figure 1.1).
- Self/Mutual capacitive sensors
- Sensor flexibility
  - Automatic sensor tuning for optimum sensitivity
  - Internal voltage regulator
  - Reference capacitor
  - On-chip noise filtering
  - Detection debounce and hysteresis
  - Wide range of capacitance detection
- Proximity Sensing
  - High SNR for proximity sensing
  - High parasitic load capability (400pF)
- Variance detection
  - Calculate signal variance
  - Triggers based on signal variance level
  - Variance estimates user interaction level (user movement magnitude)
- Design simplicity
  - PC GUI for obtaining optimal on-chip settings
  - One-time settings programming (during MP)
- 3x GPIO's to output status flags from any channel
- Automated system power modes for optimal response vs consumption
- I^2C communication interface with IRQ/RDY (up to fast plus -1MHz)
- Standalone, event mode (RDY based), streaming mode (RDY based) or polling communication options
- Fully customizable standalone user interface due to programmable memory
- Supply Voltage 1.8V(-5%)to 3.5V
- Small packages:
  - WLCSP18 (1.62x 1.62x0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch

RoHS2 Compliant

WLCSP18 & QFN20 package representation only

1.2 Applications

- SAR-limiting proximity sensing
- Proximity Backlighting
- Presence detection

1.3 Block Diagram

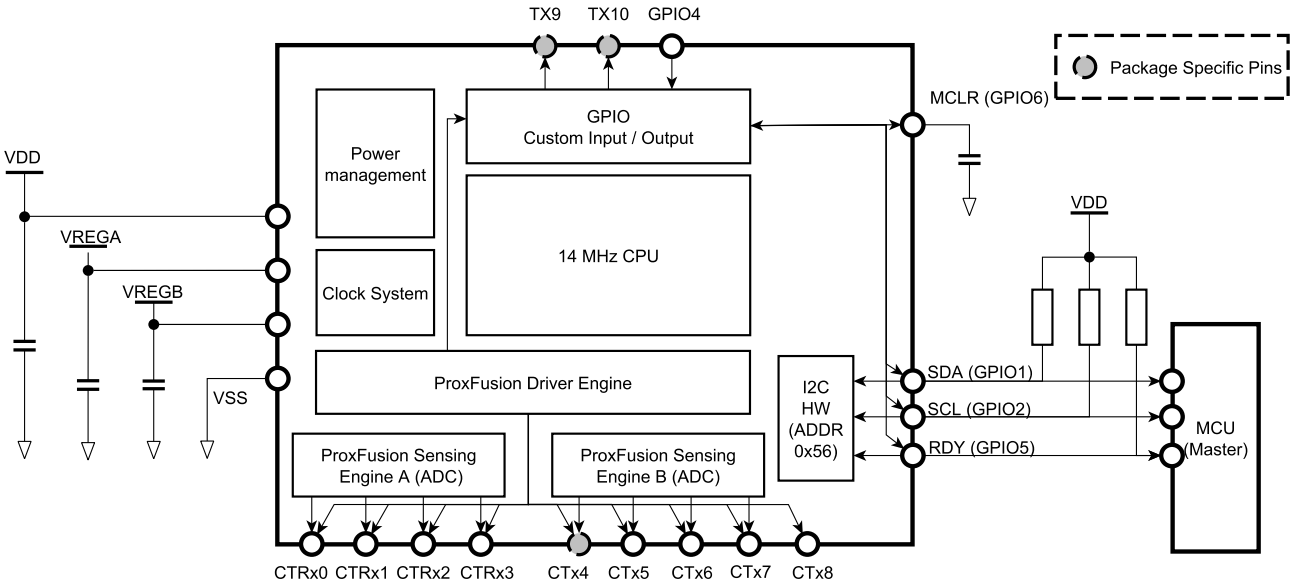


Figure 1.1: Functional Block Diagram[i]

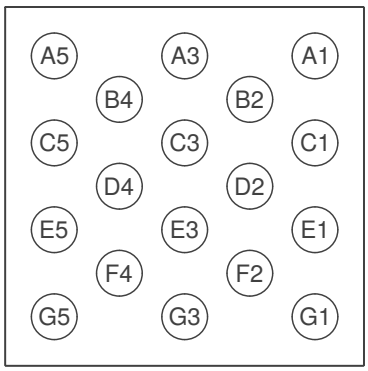
[i] WLCSP18 packages do not have a CRx4 and combines TX9 and TX10

Contents

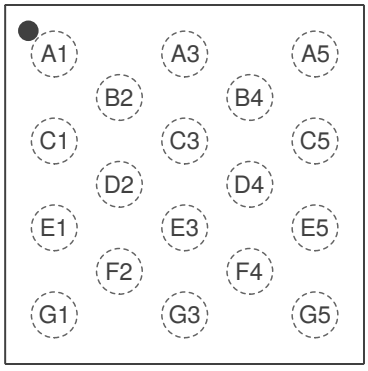
2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

Table 2.1: 18-pin WLCSP18 Package



Ball-side View

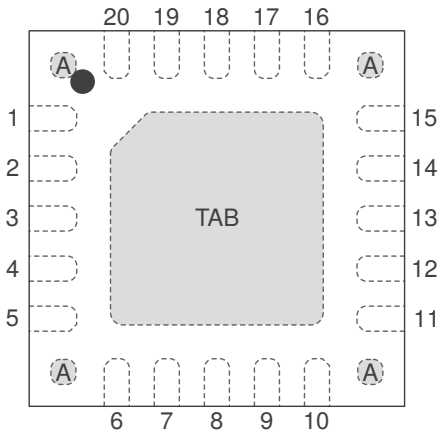


Top-side View

Pin no.	Signal
A1	CTx9/GPIO0/CTx10/GPIO3[i]
A3	SCL/GPIO2
A5	MCLR/GPIO6
B2	CTx11/GPIO4
B4	SDA/GPIO1
C1	CTx8
C3	RDY/GPIO5
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Top View

Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8
4	VREGA	14	CTx9/GPIO0
5	CRx0/CTx0	15	CTx10/GPIO3
6	CRx1/CTx1	16	CTx11/GPIO4
7	CRx2/CTx2	17	RDY/GPIO5
8	CRx3/CTx3	18	SCL/GPIO2
9	CRx4/CTx4	19	SDA/GPIO1
10	CRx5/CTx5	20	MCLR/GPIO6

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)

[i] Please note that CTx9/GPIO0 and CTx10/GPIO3 are connected together in the WLCSP18 package.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.
[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	CTx9/GPIO0	Prox/Digital		VREGA/VDD
B4	19	SDA/GPIO1	Digital		VDD
A3	18	SCL/GPIO2	Digital		VDD
A1	15	CTx10/GPIO3	Prox/Digital		VREGA/VDD
B2	16	CTx11/GPIO4	Prox/Digital		VREGA/VDD
C3	17	RDY/GPIO5	Digital		VDD
A5	20	MCLR/GPIO6	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8	C1	13	O	CTx8 pad
	CTx9/GPIO0	A1	14	IO	CTx9/GPIO0 pad
	CTx10/GPIO3	A1	15	IO	CTx10/GPIO3 pad
	CTx11/GPIO4	B2	16	IO	CTx11/GPIO4 pad
GPIO	RDY/GPIO5	C3	17	O	RDY/GPIO5 pad
	MCLR/GPIO6	A5	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA/GPIO1	B4	19	IO	I^2C data
	SCL/GPIO2	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

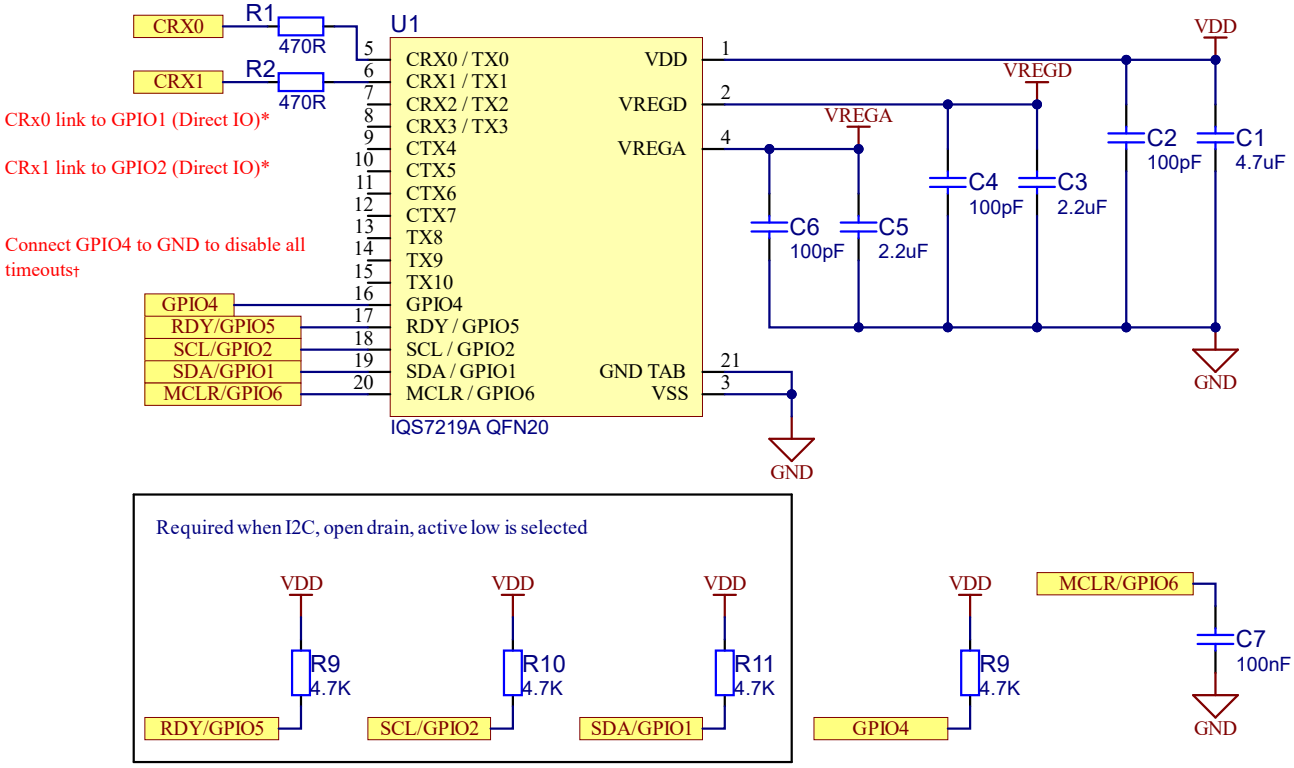


Figure 2.1: IQS7219A Self-capacitive Reference Schematic

*Output linked to CRx0 and CRx1 applicable to order code 102, 103 and 104

†GPIO4 functionality only available on order codes 104, 106 and 107. Pulling GPIO4 low, will disable all timeout functionality

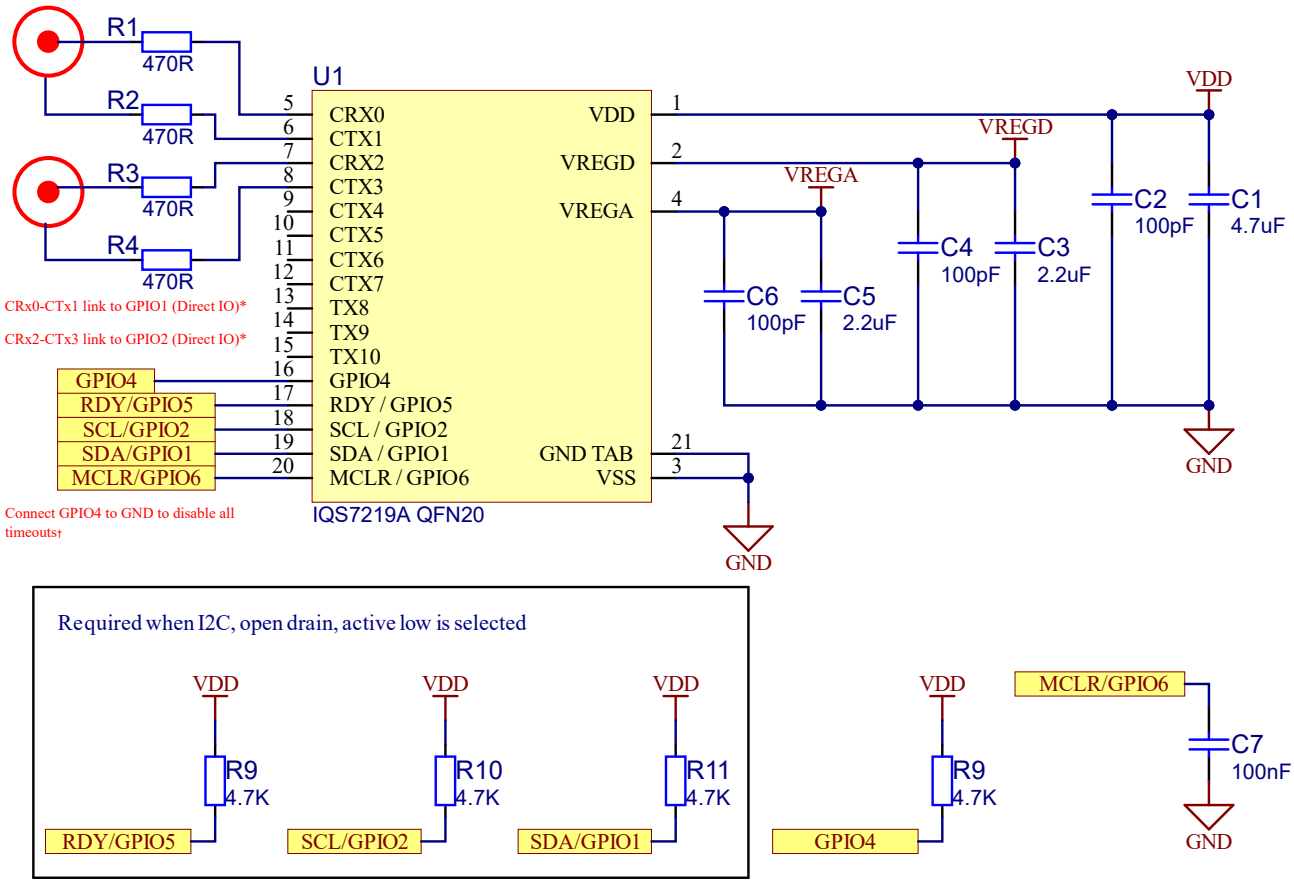


Figure 2.2: IQS7219A Mutual Capacitive Reference Schematic

*Output linked to CRx0-CTx1 and CRx2-CTx3 applicable to order code 105

†GPIO4 functionality only available on order code 106 . Pulling GPIO4 low, will disable all timeout functionality

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.5 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.5	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	2×C_{VREGA}	3×C_{VREGA}		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR≤ 200 mΩ	2	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR≤ 200 mΩ	2	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[i]	pF
$Cm_{CTx–CRx}$	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[i]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, f_{xfer} = 1 MHz Mutual-capacitance mode, f_{xfer} = 4 MHz			 100[i] 25[i]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[ii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iii]	0.47	10[iv]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iii]	0.47	10[iv]	kΩ

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[v]	±4000	V

3.4 Current Consumption

Power mode	Active channels	Sample Rate (ms)	Voltage (V)	Current [µA]
Normal Power	Two Channels	20	3.3	110
Normal Power	Two Channels	20	1.8	108

[i] RCx = 0 Ω.

[ii] Please note that the maximum values for Cp and Cm are subject to this ratio.

[iii] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[iv] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.

[v] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) – slope > 100 V/s	1.040	1.353	1.568	V
V_{VREGD}	Power-up/down level (Reset trigger) – slope > 100 V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

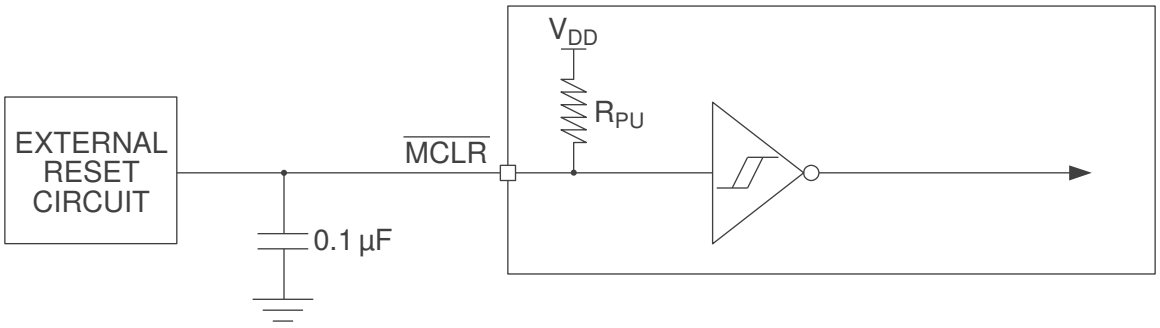


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA			0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2			V
V_{IL}	Input low voltage				VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7			V
C_{b_max}	SDA & SCL maximum bus capacitance				550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26			µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0			ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50			ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0		50	ns

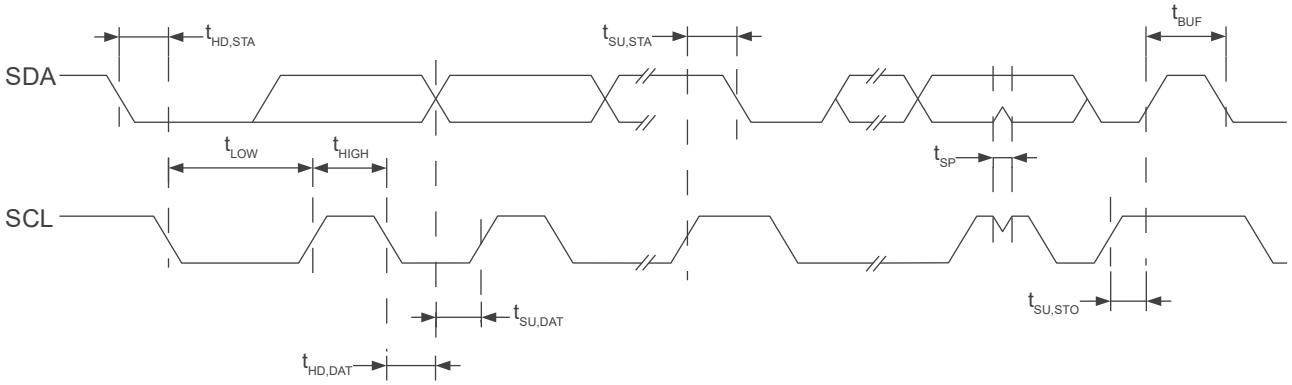


Figure 4.2: I²C Mode Timing Diagram

[i] Refers to CTx9, CTx10, CTx11, and RDY pins.

5 ProxFusion® Module

The IQS7219A contains dual ProxFusion® modules that uses patented technology to measure and process the sensor data. Multiple touch and proximity outputs are the primary output from the sensor.

5.1 Channel Options

Self-capacitance and Mutual capacitance designs are possible with the IQS7219A

- Sensor pad design overview: AZD125
- Mutual capacitive button layout guide: AZD125

5.2 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance, and all outputs are derived from this.

5.2.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *(Maximum counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.3.1 Reseed

Since the *Reference/LTA* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0x80, bit3).

5.4 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

5.5 Automatic Re-ATI

5.5.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7219A , a status bit will set momentarily to indicate that this has occurred.

5.5.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in register 0xA7, 0xB7 and 0xC7.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{8}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and that the and the default boundary value is 1/8*800 = 100. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\textbf{Reference} > \textbf{900 or Reference} < \textbf{700}$$

The ATI algorithm executes in a short time, so goes unnoticed by the user.

5.5.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6 Sensing Modes

6.1 Power Mode and Mode Timeout

The IQS7219A offers 3 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption

In order to optimize power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout". The value for the power mode to never timeout (i.e the current power mode will never progress to a lower power mode), is 0x00.

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitized raw input offers various damping options as defined in Table A.14.

Damping factor = Beta/256

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below, some are described, the other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

While *Reset* bit remains set:

- The device will not be able to enter into I^2C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared)
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

7.2.2 Software Reset

The IQS7219A can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 Automated Start-up

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up the device will automatically use the default settings and perform the configuration/setup accordingly.

8.3 RF Immunity

The IQS7219A has immunity to RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 4.7μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470Ω-1kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7219A supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7219A implements 8-bit addressing with 2 bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The default 7-bit device address is 0x56 (’1010110’). The full address byte will thus be 0xAD (read) or 0xAC (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement 16-bit addressing scheme.

9.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to only address each Block as an 8-bit address, and then continue to clock into the next address locations. For example, if the procedure depicted below is followed, you will read the values from the hypothetical address 0xE000 to 0xE300:

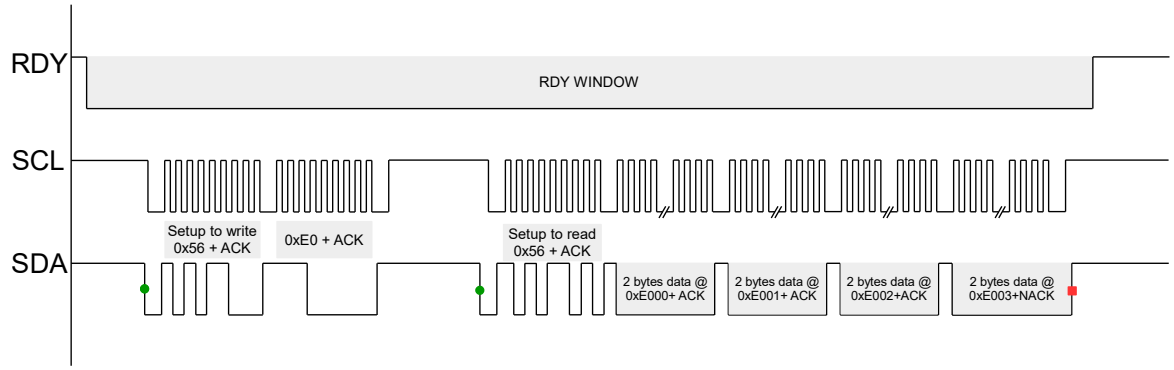


Figure 9.1: Extended 16-bit Addressing for Continuous Block

However, if you need to address a specific byte in that extended memory map space, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

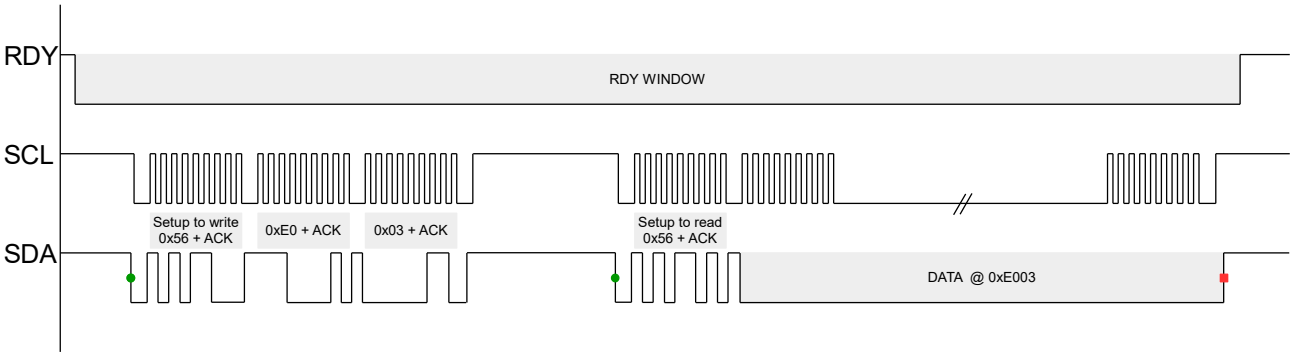


Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

The h file generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively -in a single block of data or the entire memory map, (refer to figure 9.1), or data can be written explicitly to a specific address (refer to figure 9.2). An example of the h file exported by the GUI and the order of the data, is shown in figure 9.3 below.

```
/* Change the Sensor 0 Settings */
/* Memory Map Position 0x30 - 0x39 */
#define SENSOR_0_SETUP_0                0x01
#define SENSOR_0_SETUP_1                0x07
```

Start address
LSB
MSB

Figure 9.3: Example of an H file Exported by the GUI

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive, however the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 20ms and can be adjusted in register 0x81.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 8 register 0x8D) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

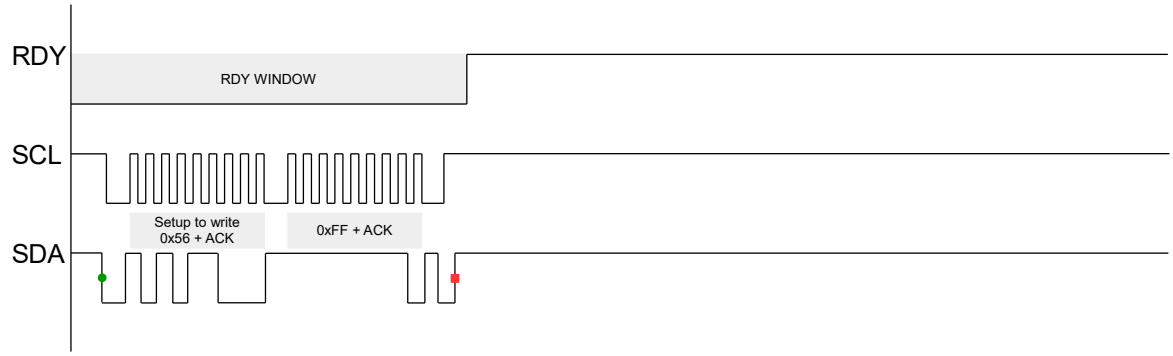


Figure 9.4: Force Stop Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

9.10 I²C Interface

The IQS7219A has 3 *I²C interface options*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0x85* (normal power), register *0x87* (low power) and register *0x89* (ultra low power)

respectively.

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.10.3 I²C Stream in Touch Mode

Stream in touch is a hybrid I²C mode between streaming mode and event mode. The device follows event mode I²C protocol but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I²C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

9.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *Events* register 0x11 to ensure all events flags are cleared otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode

9.11.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.2 and Table A.3:

- Power mode change
- Prox, touch or halt event
- ATI error
- ATI active
- ATI Event

9.11.2 Force Communication

In streaming mode, the IQS7219A I²C will provide Ready (RDY) windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7219A should only be initiated in a Ready window but a communication request described in figure 9.5 below, will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The time between the communication request and the opening of a RDY window (t_{wait}), is dependent on the report rate of the current power mode. t_{wait} can extend up to the current report rate +20% due to variability in the clock. Example, if a report rate of 100ms is chosen, the report rate may vary between 80ms and 120ms [i].

[i] Please contact Azoteq for an application specific value of t_{wait}

There is a possibility of a communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period. However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional precautionary measure, the IC can be reset using the MCLR pin and reinitialized if there is no response after a specified number of retries.

A force communication request should be avoided while RDY is in the LOW state. If a communication request is sent at the exact moment when an event causes RDY to go low, the window will close again after sending the I^2C STOP signal. In such a scenario, the device will provide an invalid communication response (0xEE) because the host is attempting to read from the device outside of a communication window (i.e. while RDY is high). To prevent this issue, it is recommended to read the product number during each ready window to ensure that the response received is valid.

A slight delay may occur in receiving an acknowledgement (ACK) when attempting force communication while the device is in an internal lower power mode with certain peripherals switched off. This delay can occur regardless of the state of the current system power mode. The communication request sequence is shown in figure 9.5 below.

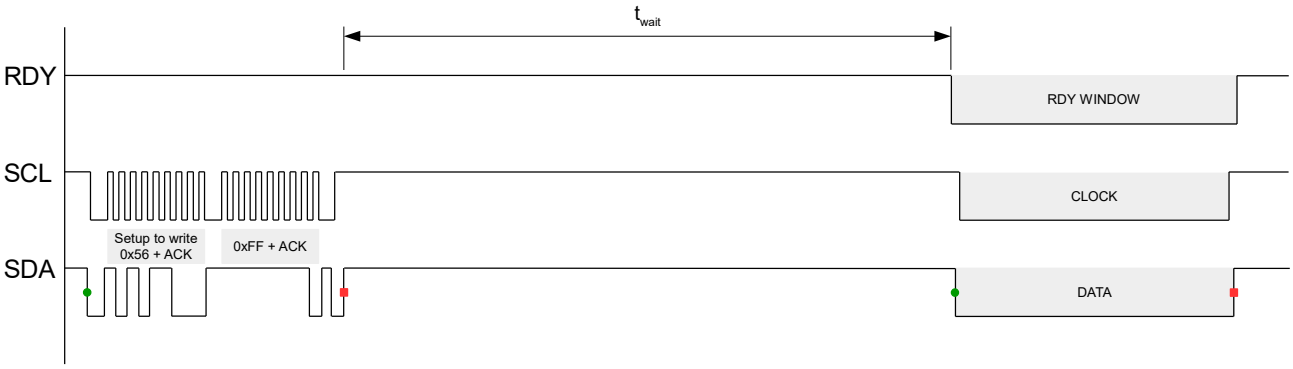


Figure 9.5: Force Communication Sequence

9.12 Program Flow Diagram

The program flow for event mode communication is shown in figure 9.6

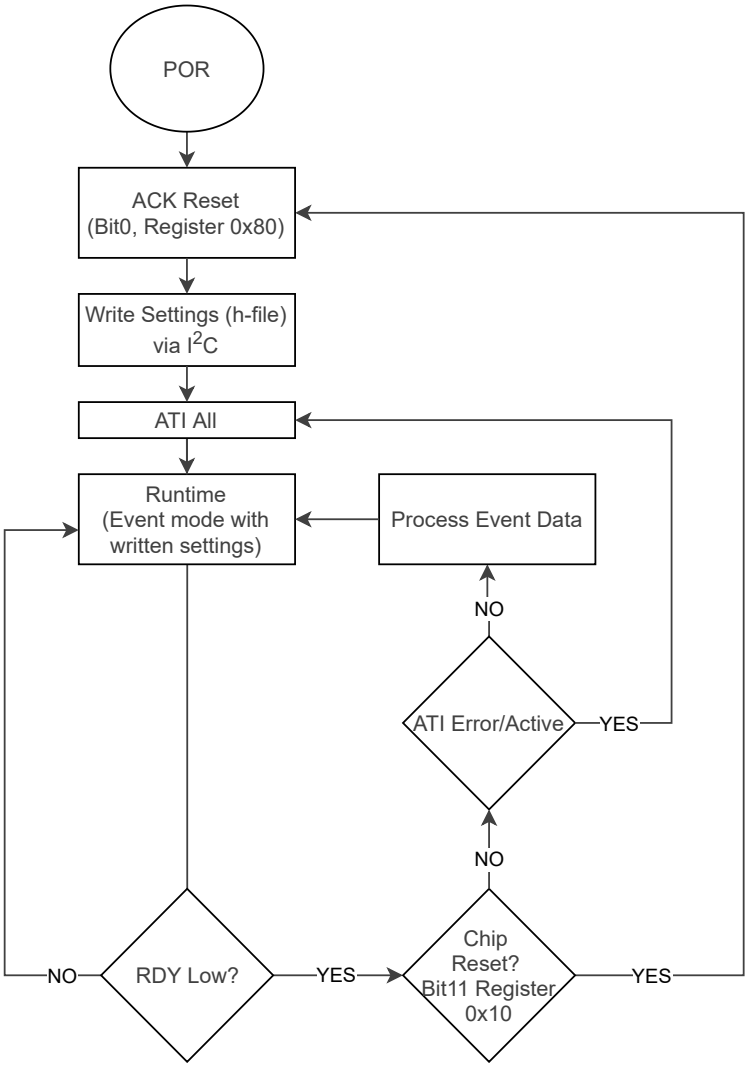


Figure 9.6: Progam Flow Diagram

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)		Notes
0x00 - 0x09	Version details		See Table A.1
Read only	**Device Status**		
0x10	System Fields		See Table A.2
0x11	PXS Status		See Table A.3
Read only	**Channel Counts**		
0x12	Channel 0 Filtered		16-bit value
0x13	Channel 0 LTA		
0x14	Channel 1 Filtered		
0x15	Channel 1 LTA		
0x16	Channel 0 Variance LSB		See Table A.4
0x17	Channel 0 Variance MSB		
0x18	Channel 1 Variance LSB		See Table A.4
0x19	Channel 1 Variance MSB		
0x1A	Channel 0 Raw		16-bit value
0x1B	Channel 1 Raw		
Read-write	**ATI Parameters**		
0x20	Reserved	Channel 0 Course Multiplier	4-bit value
0x21	Reserved	Channel 0 Course Divider	5-bit value
0x22	Reserved	Channel 0 Fine Divider	5-bit value
0x23	Reserved	Channel 0 ATI Compensation Divider	5-bit value
0x24	Channel 0 ATI Compensation		10-bit value
0x25	Reserved	Channel 1 Course Multiplier	4-bit value
0x26	Reserved	Channel 1 Course Divider	5-bit value
0x27	Reserved	Channel 1 Fine Divider	5-bit value
0x28	Reserved	Channel 1 ATI Compensation Divider	5-bit value
0x29	Channel 1 ATI Compensation		10-bit value
Read-write	**PMU and System Settings**		
0x80	System Setup and Commands		See Table A.5
0x81	I²C Transaction Timeout		See Table A.6
0x82	Retry ATI on error period		16-bit value (ms)
0x83	Minimum ATI sample period		16-bit value (ms)
0x84	Normal Power Mode Timeout		16-bit value (ms)
0x85	Normal Power Mode Report Rate		16-bit value (ms) Range: 0 - 3000
0x86	Low Power Mode Timeout		16-bit value (ms)
0x87	Low Power Mode Report Rate		16-bit value (ms) Range: 0 - 3000
0x88	Ultra Low Power Mode Timeout		16-bit value (ms)
0x89	Ultra Low Power Mode Report Rate		16-bit value (ms) Range: 0 - 3000
Read-write	**PXS Settings**		
0x8A	Cycle 0 Mode and Channel Select		See Table A.7
0x8B	Cycle 1 Mode and Channel Select		See Table A.7
0x8C	Mutual and Self Mode Settings		See Table A.8
0x8D	I²C Settings		See Table A.9
Read-write	**Channel 0 Detection Settings**		
	Halt Detection Settings		

0x90	Active State Timeout		16-bit value (ms)
0x91	Hysteresis		See Table A.10
0x92	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0x93	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0x94	Reserved	GPIO Select	See Table A.12
	Proximity Detection Settings		
0x95	Active State Timeout		16-bit value (ms)
0x96	Hysteresis		See Table A.10
0x97	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0x98	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0x99	Reserved	GPIO Select	See Table A.12
	Touch Detection Settings		
0x9A	Active State Timeout		16-bit value (ms)
0x9B	Hysteresis		See Table A.10
0x9C	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0x9D	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0x9E	Reserved	GPIO Select	See Table A.12
Read-write	**Channel 0 PXS and ATI Settings**		
0xA0	General Settings		See Table A.13
0xA1	Filter Betas		See Table A.14
0xA2	Conversion Period	Frequency Fraction	See Table A.15
0xA3	CRx Selection		See Table A.16
0xA4	CTx Selection		See Table A.17
0xA5	ATI Base		16-bit value Range: 0 - 500
0xA6	ATI Target		16-bit value Range: 0 - 4000
0xA7	Re-ATI Band		16-bit value Range: 0 - 1500
0xA8	ATI Mode		See Table A.18
0xA9	Course Divider Preload	Fine Divider Preload	8-bit value
0xAA	Compensation Preload		10-bit value
0xAB	Variance Threshold		16-bit value
0xAC	Reserved	Fast filter band	8-bit value
Read-write	**Channel 1 Detection Settings**		
	Halt Detection Settings		
0xB0	Active State Timeout		16-bit value (ms)
0xB1	Hysteresis		See Table A.10
0xB2	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0xB3	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0xB4	Reserved	GPIO Select	See Table A.12
	Proximity Detection Settings		
0xB5	Active State Timeout		16-bit value (ms)
0xB6	Hysteresis		See Table A.10
0xB7	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0xB8	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0xB9	Reserved	GPIO Select	See Table A.12
	Touch Detection Settings		
0xBA	Active State Timeout		16-bit value (ms)
0xBB	Hysteresis		See Table A.10

0xBC	Threshold		$\frac{LTA}{2^{16}} * 16\text{-bit value}$
0xBD	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.11
0xBE	Reserved	GPIO Select	See Table A.12
Read-write	**Channel 1 PXS and ATI Settings**		
0xC0	General Settings		See Table A.13
0xC1	Filter Betas		See Table A.14
0xC2	Conversion Period	Frequency Fraction	See Table A.15
0xC3	CRx Selection		See Table A.16
0xC4	CTx Selection		See Table A.17
0xC5	ATI Base		16-bit value Range: 0 - 500
0xC6	ATI Target		16-bit value Range: 0 - 4000
0xC7	Re-ATI Band		16-bit value Range: 0 - 1500
0xC8	ATI Mode		See Table A.18
0xC9	Course Divider Preload	Fine Divider Preload	8-bit value
0xCA	Compensation Preload		10-bit value
0xCB	Variance Threshold		16-bit value
0xCC	Reserved	Fast filter band	8-bit value

11 Implementation and Layout

11.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

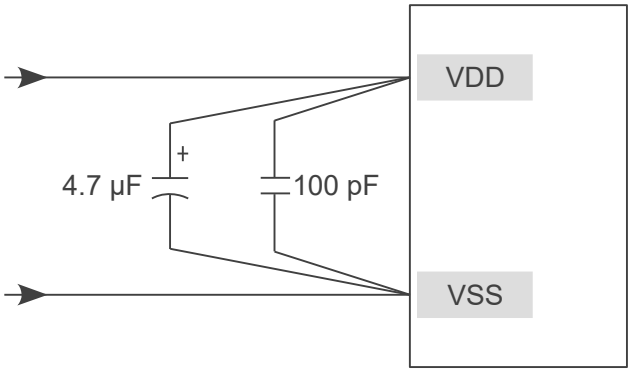


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. The figure below shows an example placement of the VREG capacitors.

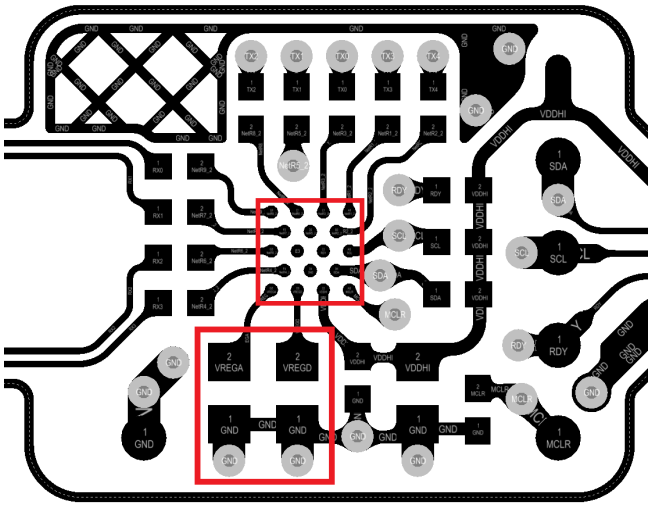


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

12 Ordering Information

12.1 Ordering Code

	IQS7219A		zzz	ppb
IC NAME	IQS7219A	=	IQS7219A	
POWER-ON CONFIGURATION	zzz	=	001	Reserved
		=	002	Reserved
		=	100	I^2C - Initialize from MCU
		=	101	Reserved
		=	102	Sensitive[i], 2 channel self-capacitance
		=	103	Sensitive Max[ii], 2 channel self-capacitance
		=	104	Sensitive[i] + Movement (variance), 2 channel self-capacitance
		=	105	Sensitive[i], 2 channel mutual-capacitance
		=	106	Sensitive[i] + Movement (variance), 2 channel self-capacitance, ability to disabled timeouts by connecting GPIO4 to GND
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

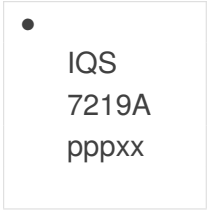
Figure 12.1: Order Code Description

12.2 Top Marking

12.2.1 WLCSP18 Package

Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 1



Product Name
ppp = product code
xx = batchcode

12.2.3 QFN20 Package Marking Option 2

Product Name
ppp = product code
xx = batchcode

[i] Base: 100, ATI target: 1000, Proximity Threshold: 10
[ii] Base: 75, ATI target: 1000, Proximity Threshold: 10

13 Package Specification

13.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

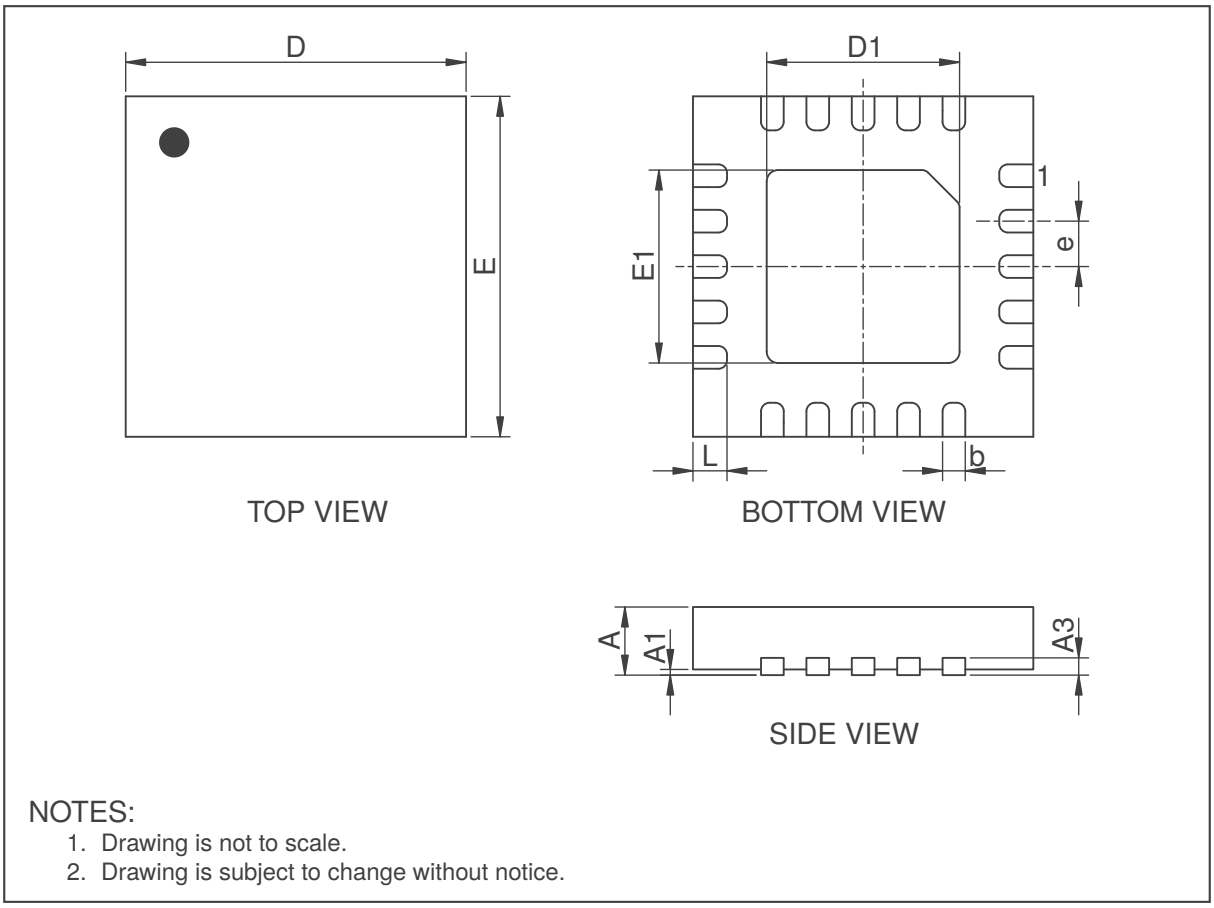
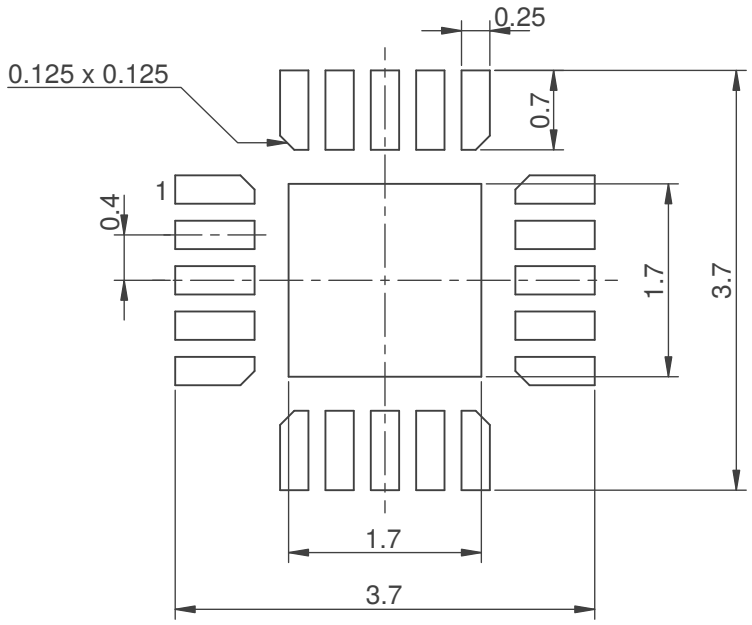


Figure 13.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

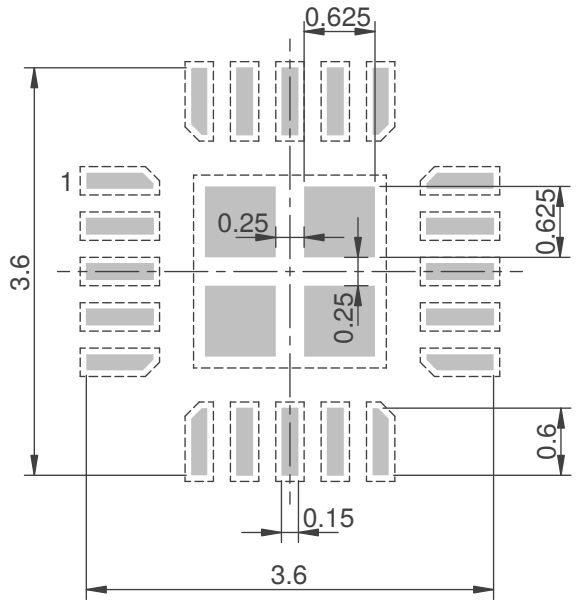
Table 13.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

13.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: QFN (3x3)-20 (QFR) Recommended Footprint

13.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

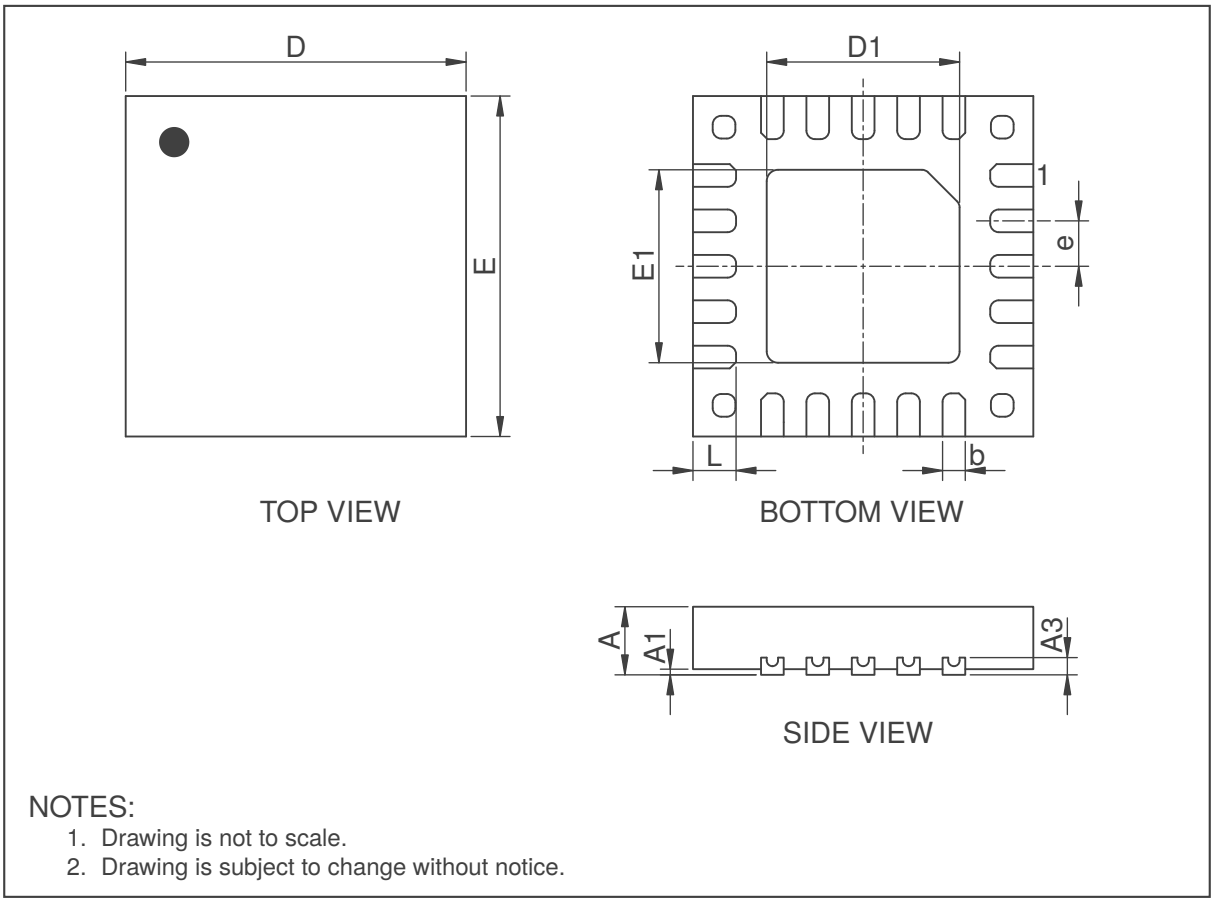
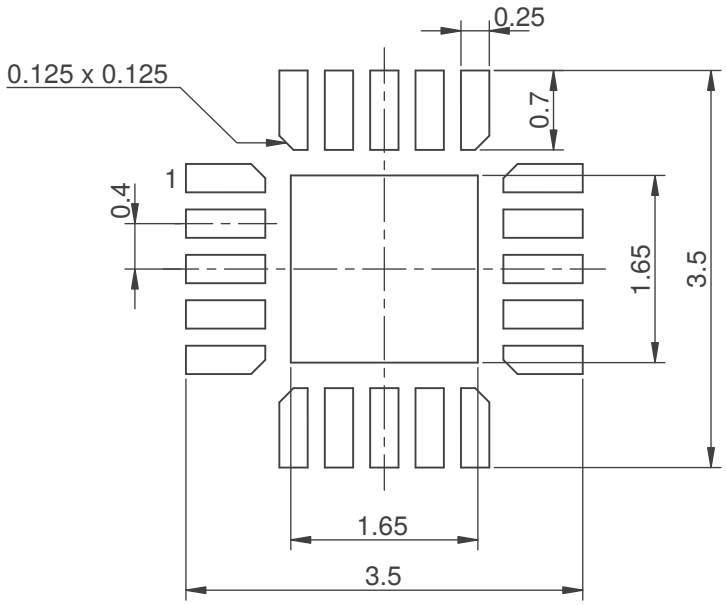


Figure 13.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

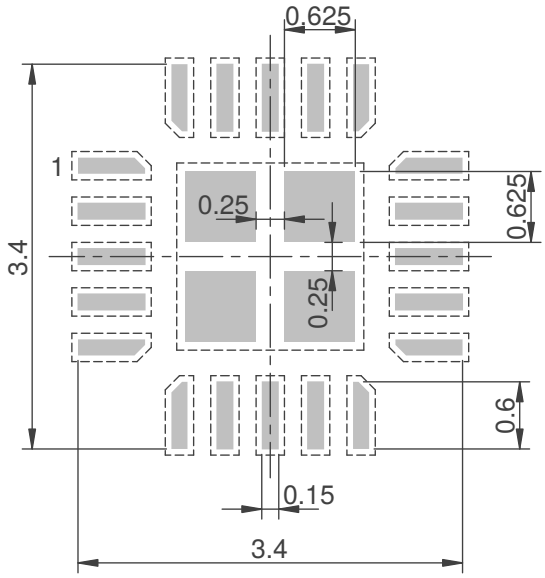
Table 13.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

13.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.4: QFN (3x3)-20 (QNR) Recommended Footprint

13.5 Package Outline Description – WLCSP18

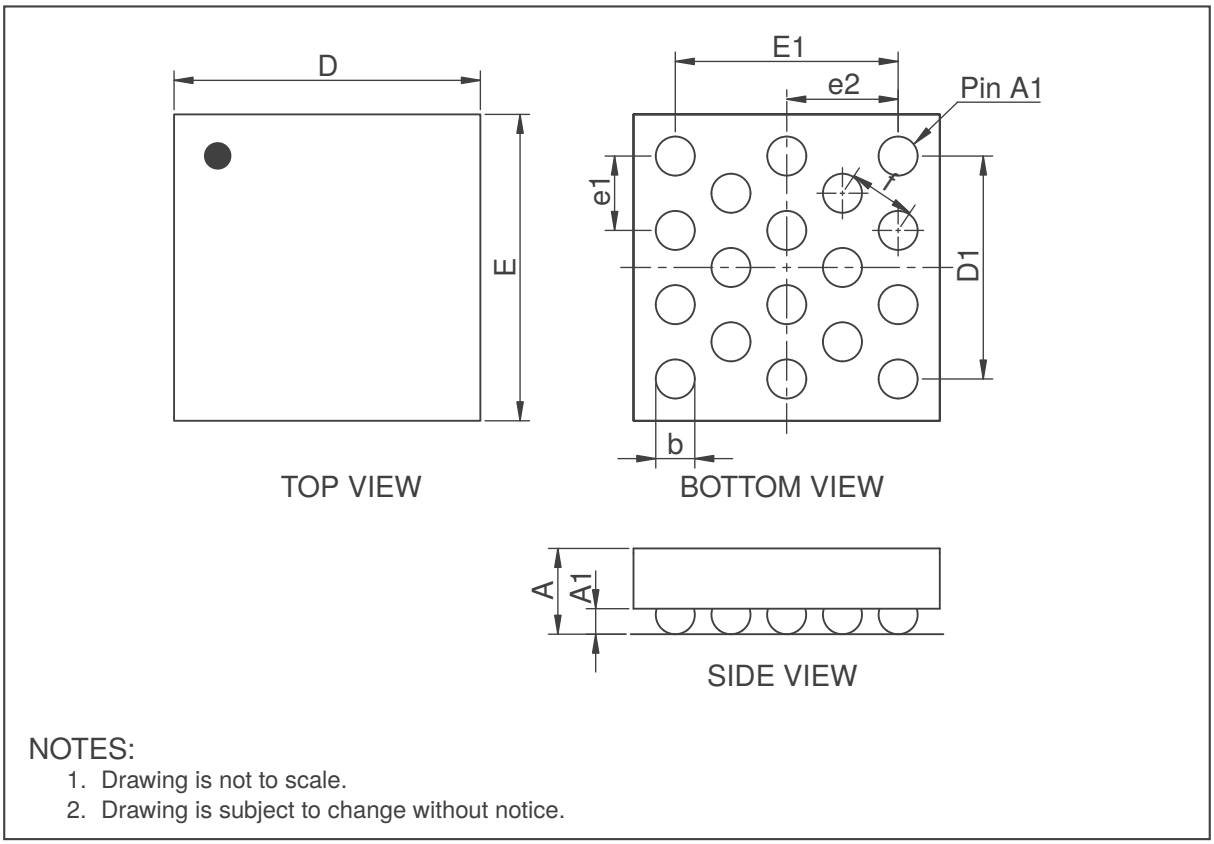
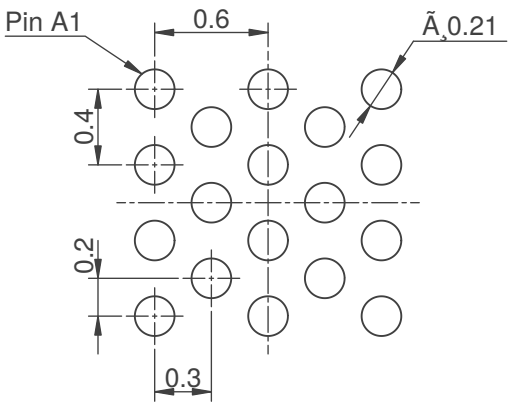


Figure 13.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

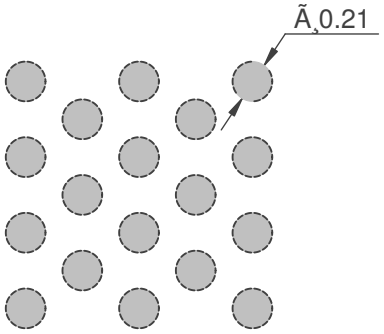
Table 13.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1		1.200 BSC	
E1		1.200 BSC	
e1		0.400 BSC	
e2		0.600 BSC	
f		0.360 REF	

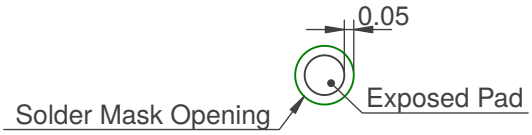
13.6 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



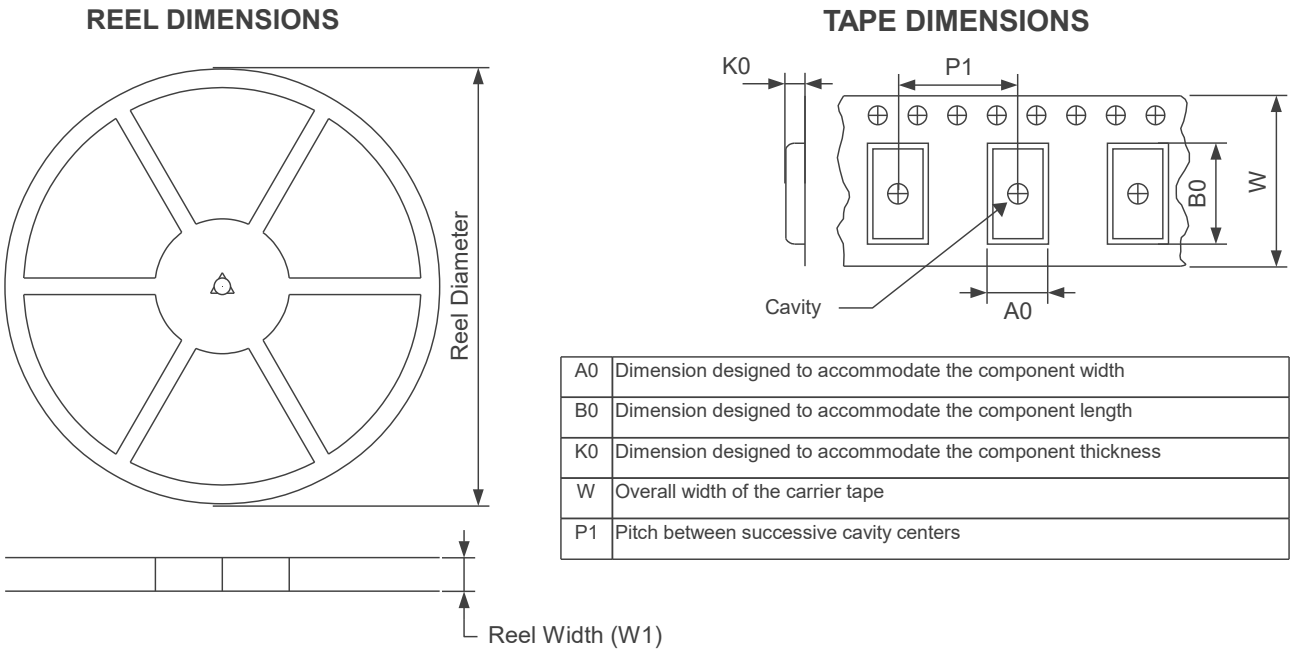
SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.6: WLCSP18 Recommended Footprint

13.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 13.7: Tape and Reel Specification

Table 13.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

13.8 Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Table A.1: Version Information

Address	Category	Name	Value
0x00	Application Version Info	Product Number	685
0x01		Major Version	1
0x02		Minor Version	12 and up
0x03		Patch Number (Commit hash)	Value between 0 and 65536
0x04			

Table A.2: System Fields

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Mode		Device Reset	Res	ATI Error	ATI Active	Reserved			Power Event	ATI Event	Touch Event	Prox Event	Halt Event

- Bit 12-13: **Power Mode**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra-Low Power
  - 11: Automatic power mode switch
- Bit 11: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 9: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 8: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 4: **Power Event**
  - 0: No power event occurred
  - 1: Power event occurred
- Bit 3: **ATI Event**
  - 0: No ATI event occurred
  - 1: ATI event occurred
- Bit 1: **Touch Event**
  - 0: No Touch event occurred
  - 1: Touch event occurred
- Bit 1: **Proximity Event**
  - 0: No Proximity event occurred
  - 1: Proximity event occurred
- Bit 0: **Halt Event**
  - 0: No Halt event occurred
  - 1: Halt event occurred

Table A.3: PXS Status

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								CH0 Vari-ance	CH1 Touch	CH1 Prox	CH1 Halt	CH0 Vari-ance	CH0 Touch	CH0 Prox	CH0 Halt

- Bit 7: **CH1 Variance**
  - 0: No variance/movement event occurred on Channel 1

- 1: Variance/movement event occurred on Channel 1

- Bit 6: **CH1 Touch**
  - 0: No Touch event occurred on Channel 1
  - 1: Touch event occurred on Channel 1
- Bit 5: **CH1 Proximity**
  - 0: No Proximity event occurred on Channel 1
  - 1: Proximity event occurred on Channel 1
- Bit 4: **CH1 Halt**
  - 0: No Halt event occurred on Channel 1
  - 1: Halt event occurred on Channel 1
- Bit 3: **CH0 Variance**
  - 0: No variance/movement event occurred on Channel 0
  - 1: Variance/movement event occurred on Channel 0
- Bit 2: **CH0 Touch**
  - 0: No Touch event occurred on Channel 0
  - 1: Touch event occurred on Channel 0
- Bit 1: **CH0 Proximity**
  - 0: No Proximity event occurred on Channel 0
  - 1: Proximity event occurred on Channel 0
- Bit 0: **CH0 Halt**
  - 0: No Halt event occurred on Channel 0
  - 1: Halt event occurred on Channel 0

Table A.4: Channel Variance

Register: 0x16, 0x17, 0x18, 0x19

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16 Bit Value															

- Bit 0-15: **Channel Variance**
  - 0: Variance channel is disabled and signal variance will not reset timer
  - 16-Bit value: Signal variance trigger size

Table A.5: System Setup and Commands

Register: 0x80

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						NP Segment Rate		Interface Selection		Power Mode Selection		Reseed	ATI	Reset	Ack reset

- Bit 8-9: **Normal Power Segment Rate**
  - 00: Every 4 Cycles
  - 01: Every 8 Cycles
  - 10: Every 16 Cycles
  - 11: Every 32 Cycles
- Bit 6-7: **Interface Selection**
  - 00: I^2C streaming
  - 01: I^2C event mode
  - 10: Standalone
  - 11: Standalone + POR I^2C
- Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Ultra low power mode
  - 11: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI

- 1: ATI

- Bit 1: **Reset Device Command**
  - 0: Do not reset device
  - 1: Reset device
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.6: I²C Transaction Timeout

Register:	0x81														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								I²C Transaction Timeout							

- Bit 0 - 7: **I²C Transaction Timeout**
  - 8-bit value [ms]
  - Range: 0 - 255
  - Default: 20ms

Table A.7: Cycle Settings

Register:	0x8A, 0x8B														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Selected Channel Number								Reserved						PXS Mode	

- Bit 8-15: **Selected Channel Number**
  - 0: Channel 0
  - 1: Channel 1
  - 255: None
- Bit 0-1: **PXS Mode**
  - 00: Self-Capacitance
  - 11: Mutual Capacitance

Table A.8: Mutual and Self Capacitance Settings

Register:	0x8C														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Self-Capacitance								Mutual Capacitance							
Res	Vref 0.5V	Res	CS 80pF	Reserved		Max Counts		Res	Vref 0.5V	Res	CS 80pF	Projected Bias Select		Max Counts	

- Bit 12 & Bit 4: **Cs 80pF cap**
  - 0: 40pF
  - 1: 80pF
- Bit 8-9 & Bit 0-1: **Maximum Counts**
  - Please note that the ATI target must be lower than the selected maximum counts value.
  - For maximum counts values higher than 4095, the ATI band must be increased to at least 500.
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-3: **Projected Bias Selection**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.9: I²C Settings

Register: 0x8D

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Res	Res	Res	Res	Res	Res	Read write check	Stop bit	Res	Res	Res	Power event mask	ATI event mask	Touch event mask	Prox event mask	Halt event mask

- Bit 9: **Read write check disable**
  - 0: Write not allowed to read only registers
  - 1: Read and write allowed to read only registers
- Bit 8: **Stop bit disabled**
  - 0: I²C communication window terminated by stop bit.
  - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window
- Bit 4: **Power event**
  - 0: Power event masked
  - 1: Power event enabled
- Bit 3: **ATI event**
  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 2: **Touch event**
  - 0: Touch event masked
  - 1: Touch event enabled
- Bit 1: **Prox event**
  - 0: Prox event masked
  - 1: Prox event enabled
- Bit 0: **Halt event**
  - 0: Halt event masked
  - 1: Halt event enabled

Table A.10: Hysteresis

Register: 0x91, 0xB1

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hysteresis															

- Bit 0-15: **Hysteresis Value**
  - 16 -bit value
  - Release threshold = $\frac{LTA}{2^{16}} * (\text{touch\_threshold} * (1 - \frac{\text{hysteresis\_value}}{2^{16}}))$

Table A.11: Debounce Thresholds

Register: 0x93, 0xB3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Debounce Deactivation Threshold								Debounce Activation Threshold							

- Bit 8-15: **Debounce Deactivation Threshold**
  - 8bit value
- Bit 0-7: **Debounce Activation Threshold**
  - 8bit value

Table A.12: GPIO Selection

Register: 0x94, 0xB4

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								GPIO Select							

- Bit 0-7: **GPIO Output Selection**
  - GPIO selection is only applicable to standalone mode as GPIO1 and GPIO2 are used as SDA and SCL in I²C mode.
  - 0x00: None

- 0x02: GPIO1 Push-Pull, Active Low
- 0x04: GPIO2 Push-Pull, Active Low
- 0x20: GPIO5 Push-Pull, Active Low
- 0x03: GPIO1 Active High
- 0x05: GPIO2 Active High
- 0x21: GPIO5 Active High
- 0x0A: GPIO1 Open Drain
- 0x0C: GPIO2 Open Drain
- 0x28: GPIO5 Open Drain

Table A.13: General Channel Settings

Register: 0xA0, 0xC0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power Counts Filter				Normal Power Counts Filter				Res-erved	Direct state ma-chine[i]	Touch LTA	Prox LTA	Halt LTA	Res	Direc-tion	Dual

- Bit 12-15: **Low Power Counts Beta Filter**
  - 4-bit value
- Bit 8-11: **Normal Power Counts Beta Filter**
  - 4-bit value
- Bit 6: **Enable Directionality state machine** [i]
  - 0: Directionality state machine disabled
  - 1: Directionality state machine enabled
- Bit 5: **Touch is LTA Dependent**
  - Touch threshold is set in registers 0x9C and 0xBC
  - 0: Disabled: threshold = 16-bit threshold value
  - 1: Enabled: threshold = $\frac{\text{LTA}}{2^{16}} * \text{16-bit threshold value}$
- Bit 4: **Proximity is LTA Dependent**
  - Proximity threshold is set in registers 0x97 and 0xB7
  - 0: Disabled: threshold = 16-bit threshold value
  - 1: Enabled: threshold = $\frac{\text{LTA}}{2^{16}} * \text{16-bit threshold value}$
- Bit 3: **Filter Halt is LTA Dependent**
  - Halt threshold is set in registers 0x92 and 0xB2
  - 0: Disabled: threshold = 16-bit threshold value
  - 1: Enabled: threshold = $\frac{\text{LTA}}{2^{16}} * \text{16-bit threshold value}$
- Bit 1: **Detection Direction**
  - 0: Detect in negative direction (Counts < LTA)
  - 1: Detect in positive direction (Counts > LTA)
- Bit 0: **Dual Directional Sensing**
  - 0: Dual directional sensing disabled
  - 1: Dual directional sensing enabled
  - Ignores Bit 1 when enabled

Table A.14: Filter Betas

Register: 0xA1, 0xC1

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power Fast LTA Filter				Normal Power Fast LTA Filter				LTA Low Power LTA Filter				LTA Normal Power LTA Filter			

- Bit 12-15: **Low Power LTA Fast Beta Filter Value**
  - 4-bit value
- Bit 8-11: **Normal Power LTA Fast Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Low Power LTA Beta Filter Value**
  - 4-bit value

[i] Only available on order code 100 and 105; Reserved bit on all other order codes

- Bit 0-3: **Normal Power LTA Beta Filter Value**
  - 4-bit value

Table A.15: Conversion Frequency

Register:	0xA2, 0xC2															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Period								Frequency Fraction							

- Bit 8-15: **Conversion Period**
  - $\frac{128}{FrequencyFraction} - 2$
  - Range: 0 - 127
- Bit 0-7: **Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 255

Table A.16: CRx Selection

Register:	0xA3, 0xC3															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				RX3	RX2	RX1	RX0	Frequency prescalar							

- Bit 11: **Rx3**
  - 0: Rx3 disabled
  - 1: Rx3 enabled
- Bit 10: **Rx2**
  - 0: Rx2 disabled
  - 1: Rx2 enabled
- Bit 9: **Rx1**
  - 0: Rx1 disabled
  - 1: Rx1 enabled
- Bit 8: **Rx0**
  - 0: Rx0 disabled
  - 1: Rx0 enabled
- Bit 0-7: **Conversion Frequency Prescalar**
  - 00: $F_{OSC}/1$
  - 01: $F_{OSC}/2$
  - 10: $F_{OSC}/4$
  - 11: $F_{OSC}/8$

Table A.17: CTx Selection

Register:	0xA4, 0xC4															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

- Bit 8: **Tx8**
  - 0: Tx8 disabled
  - 1: Tx8 enabled
- Bit 7: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 6: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 5: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 4: **Tx4**
  - 0: Tx4 disabled

- 1: Tx4 enabled

- Bit 3: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 2: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 1: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 0: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled

Table A.18: ATI Mode

Register:		0xA8, 0xC8													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved													ATI Mode		

- Bit 0-2: **ATI Mode**
  - 000: Disabled
  - 001: Compensation only
  - 010: From compensation Divider
  - 011: From fine fractional divider
  - 100: From course fractional divider
  - 101: Full

B Revision History

Release	Date	Changes
v1.0	November 2021	Initial release
v1.1	November 2021	Reference schematic updated to show IO links
v1.2	January 2022	Power mode bit definition updated
v1.3	January 2022	Added order code 106
v1.4	April 2022	I^2C information added Memory map updates
v1.5	January 2024	Added revision history Added order code 002 Updated power mode and mode timeout section Updated force communication description Updated channel options section

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